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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,915	12/14/2001	David Meltzer	ERD01-001	9628
20178	7590	09/28/2005	EXAMINER	
EPSON RESEARCH AND DEVELOPMENT INC INTELLECTUAL PROPERTY DEPT 150 RIVER OAKS PARKWAY, SUITE 225 SAN JOSE, CA 95134			GHULAMALI, QUTBUDDIN	
			ART UNIT	PAPER NUMBER
			2637	

DATE MAILED: 09/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/016,915	MELTZER, DAVID	
	Examiner	Art Unit	
	Qutub Ghulamali	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 14 December 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-56 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 37-47 is/are allowed.
- 6) ☒ Claim(s) 1, 2, 4-11, 13-20, 22-36, 48-56 is/are rejected.
- 7) ☒ Claim(s) 3, 12 and 21 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>2/26/02</u> .   | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Specification*

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

In the instant case the Abstract of the Disclosure exceeds the range of 50 to 150 words. Appropriate correction is required to contain the Abstract within the guidelines.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1, 2, 4-11, 13-20, 22-36, 48-56, are rejected under 35 U.S.C. 103(a) as being unpatentable over Chiueh et al (USP 6,674,824) in view of Thompson (USP 4,499,434).

Regarding claims 10 and 16, Chiueh discloses all limitations of the claims 10 and 16. Chiueh, however, does not explicitly disclose a lock detection circuit to detect loss of phase-frequency lock of the output frequency signal of said phase lock loop with the input reference signal and upon detection of said loss of phase-frequency lock provide an unlock alarm.

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Thompson in a similar field of endeavor discloses a lock limit comparator (lock detector, 20) to detect loss of phase-frequency lock of the output frequency signal of said phase lock loop with the input reference signal and upon detection of said loss of phase-frequency lock provide an unlock alarm (col. 3, lines 3-17, 31-50, 61-67; col. 5, lines 26-58). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a lock detection means to detect the loss of phase and provide an alarm as taught by Thompson in the system of Chiueh because it can provide synchronization (loss of synchronization) status of phase lock loop.

Regarding claims 2, 11, 20, 29, 30 and 50, Chiueh discloses all limitations of the claims above. Chiueh, however, does not explicitly disclose a latching circuit in communication with the second logic function and the input reference signal to indicate an unlock alarm at loss of phase lock. However, Thompson in a similar field of endeavor discloses (fig. 1) a latching circuit in communication with the second logic function and the input reference signal to capture and retain said error signal to provide an unlock alarm signal indicating loss of phase-frequency lock of said phase lock loop (col. 3, lines 62-64; col. 5, lines 35-53). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include in the circuit of Chiueh, a latching circuit, to provide an unlock alarm signal indicating loss of phase-frequency lock as taught by Thompson, because it can indicate an error condition in receiver susceptible to phase noises.

Regarding claim 49, Chiueh discloses all limitations of the claims above. Chiueh, however, does not explicitly disclose capturing and retaining unlock alarm signal for transfer to external circuitry. Thompson in a similar field of endeavor discloses (fig. 1) steps of capturing

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and retaining unlock alarm signal for transfer to external circuitry (col. 5, lines 35-58). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use steps of capturing and retaining unlock alarm signal for transfer to external circuitry as taught by Thompson in the circuit of Chiueh, because it can facilitate the transfer of an alarm signal to external circuitry when needed enhancing the receivers operational characteristics.

Regarding claims 19, 25, 28 and 34, Chiueh and Thompson in combination disclose all of the claimed limitations of the claim except a clock extractor to remove said timing signal from said data stream. The clock extraction from transmission signals is well known in the art of communications systems wherein a clock is embedded in a digital data stream to be extracted and well documented and therefore quite obvious to a person of ordinary skill in the art (see references; Casper et al (USP 5,963,608) and Yousefi et al (USP 5,448,598)).

Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chiueh et al (USP 6,674,824) in view of Thompson (USP 4,499,434) and further in view of Casper et al (USP 5,963,608) and Yousefi et al (USP 5,448,598).

Regarding claim 1, Chiueh discloses a lock detection circuit in communication with a phase lock loop to detect phase-frequency lock of an output frequency signal of said Phase Lock Loop with an input reference signal, comprising:

a first logic function circuit to combine a frequency increase signal and a frequency decrease signal of said phase lock loop to provide a frequency deviation signal (fig. 1; col. 5, lines 2-10, ; and

a second logic function circuit to combine the frequency deviation signal with the input reference signal to determine that the frequency deviation signal has a greater duration than a portion of a

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cycle of said input reference signal and provide an error signal (fig. 1; col. 1, lines 41-51; col. 6, lines 7-40).

Regarding claims 4, 13, 22, 31, Chiueh discloses a programmable frequency divider (6), connected to receive the input reference signal, divide said input reference signal, and transfer the divided input reference signal to the second function circuit, wherein said second logic function circuit combines the deviation signal and the divided input reference signal to generate the error signal (fig. 1; col. 4, lines 48-51; col. 5, lines 53-67; col. 6, lines 1-6).

Regarding claims 5, 6, 8, 9, 14, 15, 17, 18, 23, 24, 26, 27, 32, 33, 35, 36, 52, 52, 55 and 56, Chiueh discloses first logic function and a second logic function is an OR gate and an AND gate (figs 2, 4(a), 6; col. 6, lines 10-32, 41-60).

Regarding claims 7 and 48, Chiueh discloses a lock detection circuit in communication with a phase lock loop to detect phase-frequency lock of an output frequency signal of said Phase Lock Loop with an input reference signal, comprising:

a phase-frequency detector in communication with the phase lock loop to receive the output frequency signal and the input reference signal to generate a frequency increase signal (UP) and a frequency decrease signal (DN) indicative of an amount of phase-frequency deviation of the output frequency signal has from the input reference signal (col. 4, lines 44-51; col. 5, lines 3-14; col. 6, lines 7-32);

a first logic function circuit to combine a frequency increase signal and a frequency decrease signal of said phase lock loop to provide a frequency deviation signal (fig. 1; col. 5, lines 2-10);  
and

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a second logic function circuit to combine the frequency deviation signal with the input reference signal to determine that the frequency deviation signal has a greater duration than a portion of a cycle of said input reference signal and provide an error signal (fig. 1; col. 1, lines 41-51; col. 6, lines 7-40).

As per claim 54, the steps claimed as method is nothing more than restating the function of the specific components of the apparatus claimed above and therefore, it would have been obvious, considering the aforementioned rejection for the apparatus claims 19, 25, 28 and 34.

#### *Allowable Subject Matter*

4. Claims 37-47 allowed.
5. Claims 3, 12 and 21, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### *Conclusion*

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patents:

Wolaver (USP 4,590,602) discloses a wide range clock recovery circuit with lock detector.

Masuda et al (USP 4,366,478) shows a signal transmitting and receiving apparatus.

Park (USP 5,673,004) discloses a method and circuit for controlling digital processing Phase-Locked Loop for network synchronization.

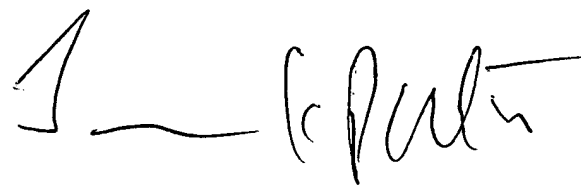
Casper et al (USP 5,963,608) discloses clock extraction for high speed variable data rate communication system.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutub Ghulamali whose telephone number is (571) 272-3014. The examiner can normally be reached on Monday-Friday from 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QG.  
September 21, 2005.

A handwritten signature in black ink, appearing to read 'Jay K. Patel', with a stylized flourish at the end.

**JAY K. PATEL**  
**SUPERVISORY PATENT EXAMINER**